ABSTRACT

A latency-independent interface between hardware components, such as a hard disk controller (HDC) and a read/write (R/W) channel or a read channel (RDC) supports high read and write latencies of greater than one sector. Such an interface also supports a split sector format and multiple mark format. In addition to read and write clock signals, the interface comprises a data gate signal that controls the transfer of data between the the HDC and R/W channel, and a media gate signal that controls transfer of mode selection information from the HDC to the R/W channel and also controls the transfer of data between the R/W channel and a disk. The media gate signal replaces the conventional read and write gate control signals. A buffer attention signal is also provided.